Family list
1 family member for: **JP59068921**
Derived from 1 application

1 FORMATION OF THIN FILM

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EC: H01L21/20

IPC: ***H01L21/205; H01L21/20; H01L21/203*** (+

Publication info: JP59068921 A - 1984-04-19

(19) Japan Patent Office (JP)

(12) Publication of Patent Application (A)

(11) Publication Number: Japanese Published Patent Application No. S59-68921

(43) Date of Publication: April 19, 1984

(51) Int. Cl.[3]	Identification Mark	JPO File Number
H 01 L 21/20		7739-5F
21/203		7739-5F
21/205		7739-5F
21/285		7638-5F

The Number of Inventions: 1

Request for Examination: not made

(4 pages in total)

(54) Thin Film Formation Method

(21) Application Number: S57-179405

(22) Date of Filing: October 12, 1982

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Specification

1. Title of the Invention

Thin Film Formation Method

2. Scope of Claim

A method for forming a thin film, characterized in that, after a thin film is formed on the surface of a substrate by chemical vapor deposition, a thin film with a predetermined thickness is formed on a semiconductor substrate by a sputtering method using the substrate as a target.

3. Detailed Description of the Invention

Industrial Field of the Invention

The present invention relates to a thin film formation method in a manufacturing process of a semiconductor device.

Structure of Prior Art and its Problem

In the manufacturing process of a semiconductor device such as MOSLSI, for example, thin films of insulator, semiconductor, or metal are formed several times. As the formation method, a CVD method (chemical vapor deposition) under atmospheric pressure or reduced pressure, a vacuum deposition method, a sputtering method, or the like is selected depending on the kind of thin film. For example, in the manufacturing process of an Si gate MOSLSI, an SiO_2 film or a PSG (phosphosilicate glass) film is formed by a CVD method as an interlayer insulating film between a first layer wiring formed of polycrystalline Si and a second layer wiring formed of Al.

The amount of impurities which adversely affect the characteristics of MOSLSI, such as heavy metal or alkali ions, contained in an SiO_2 film or a PSG film formed by a CVD method is small. This is because a highly pure reactive gas such as SiH_4, O_2, or PH_3 is used in a CVD method since the gas purification is easy. On the other hand,

since the CVD method is conducted to form a thin film at low temperature, for example, 450 °C, the thin film has weak adhesion to the substrate and its density is not sufficient. Accordingly, it is necessary to perform heat treatment at high temperature close to 1000 °C in order to strengthen the adhesion and increase the density so that the film has adequate characteristics as an interlayer insulating film.

As the density of LSI becomes higher, in order to form a MOS transistor with fine dimension, it is necessary that the junction depth of source and drain be shallow. For example, in order to form a MOS transistor with the gate length of 1.5 μm, the junction depth of source and drain needs to be approximately 0.3 μm. After B is added to the source and drain regions by ion implantation, conventional heat treatment at high temperature of 1000 °C cannot be performed. Therefore, an SiO_2 film or a PSG film just formed by a CVD method as an interlayer insulating film is not adequately dense, so that the film has poor withstand voltage, impurity stopping power, alkali ion trapping force, and the like, which are required for an interlayer insulating film.

In addition, the above-described SiO_2 film or PSG film formed as an interlayer insulating film of LSI by a CVD method has poor step coverage over the underlying wirings. Therefore, an overlying wiring formed on such SiO_2 film or PSG film has small thickness at where it intersects with the underlying wiring, thin line width when forming a pattern by etching, or even easiness of breaking in a bad case. In order to solve this problem, a PSG film containing phosphorus at high concentration is formed as an interlayer insulating film and subject to heat treatment in an atmosphere containing phosphorus at 1000 °C so as to cause a flow, which means so-called reflow treatment has been conducted. However, the reflow treatment, which is heat treatment at a temperature as high as 1000 °C, also cannot be performed to form a source and drain junction that is shallow as described above; therefore, a problem such as thinning or breaking of the overlying wiring is often caused in the manufacture of a high density LSI.

As described above, in the manufacturing process of a high density LSI for which heat treatment at high temperature cannot be performed, an interlayer insulating film formed by a conventional CVD method becomes a major cause of decrease in

manufacturing yield and reliability.

Object of the Invention

It is an object of the present invention to provide a method for forming a thin film, in which the amount of impurities contained is small, having sufficiently good characteristics even without conducting heat treatment at high temperature, and a thin film forming apparatus.

Structure of the Invention

A sputtering method is one of the thin film formation methods. This is a method in which a target is bombarded with Ar ions, for example, which are accelerated by a high electric field so that the atoms constituting the target are dissociated and attached to a semiconductor substrate, for example, which is placed so as to oppose to the target; thereby, forming a thin film.

The feature of the thin film formation method of the present invention is to form a thin film on a first substrate by the above-described CVD method, then, using the first substrate with the thin film as a target, consecutively form a thin film with a desired thickness by a sputtering method on the surface of a semiconductor substrate which is placed so as to oppose to the target.

As already described, the amount of impurities contained in the thin film formed on the first substrate by a CVD method can be sufficiently small with the use of highly pure reactive gas.

On the other hand, in a sputtering method, atoms which are dissociated from the target have high energy. This is because the atoms are knocked out from the target surface by Ar ions with high energy, accelerated by a high electric field, and a thin film which is formed by attachment of these high energy atoms to a semiconductor substrate surface has a strong adhesion with respect to the semiconductor substrate and is sufficiently dense even without heat treatment at high temperature.

Therefore, as described above, the present invention is to use as a target the first substrate with the thin film in which the amount of impurities contained is small, formed on its surface by a CVD method, when a thin film with good characteristics is formed by a sputtering method. Furthermore, the first substrate which is used as the

target is set so as to oppose to a semiconductor substrate, without being contaminated from the outside after the thin film is formed.

Description of Embodiment

An embodiment of the present invention will be described hereinafter.

A cross-sectional view of a thin film formation apparatus in this embodiment is shown in FIG. 1.

The thin film formation apparatus shown in FIG. 1 has a film formation chamber 1 and a preliminary exhaust chamber 2. In the film formation chamber 1, a first substrate such as a quartz substrate 3, for example; a holding electrode 4, incorporating a heating device for heating the held quartz substrate 3 and a magnet for accelerating electrons at the time of sputtering, which holds the first substrate; a sputtering electrode 5; and an opposing electrode 6 are provided. Furthermore, a CVD reactive gas introducing pipe 7, a sputtering Ar gas introducing pipe 8, and an exhaust pipe 9 leading to an exhaust pump for exhausting the inside of the film formation chamber 1 are connected thereto.

The preliminary exhaust chamber 2 has a semiconductor substrate holder 11 on which a semiconductor substrate 10 is placed, and an exhaust pipe 12 leading to an exhaust pump is connected to the preliminary exhaust chamber 2. In addition, a door 13 is provided on a partition wall between the film formation chamber 1 and the preliminary exhaust chamber 2; and a carrier device which opens the door 13, places the semiconductor substrate 10, and carries the semiconductor substrate holder 11 from the preliminary exhaust chamber 2 to the film formation chamber 1 or vice versa is also provided.

A case where a PSG film is formed on the surface of the semiconductor substrate 10 with the use of this thin film formation apparatus will be described.

A plurality of semiconductor substrates 10 are placed on the semiconductor substrate holder 11 and set in the preliminary exhaust chamber 2. The door 13 is closed and the inside of the preliminary exhaust chamber 2 is exhausted by the exhaust pump leading to the exhaust pipe 12.

On the other hand, in the film formation chamber 1, a PSG film 14 is formed

on the surface of the quartz substrate 3 which is the first substrate by a CVD method. First, the film formation chamber 1 is exhausted until the degree of vacuum reaches 10^{-5} Torr by the exhaust pump leading to the exhaust pipe 9. In the meantime, the quartz substrate 3 held by the holding electrode 4 is heated to 350 °C by the heating device of the holding electrode 4. After that, reactive gases of SiH_4, O_2, and PH_3 are introduced from the reactive gas introducing pipe 7 and the degree of vacuum in the film formation chamber 1 becomes stable at 10 Torr, and then, high-frequency power is applied between the opposing electrode 6 and the holding electrode 4. Between these electrodes, the reactive gas molecules are excited by the high-frequency power and reactions between gases become easy to occur. As a result, an SiO_2 film formed by the reaction between SiH_4 and O_2, including P that is decomposed from PH_3 gas, is formed on the surface of the quartz substrate 3 held and heated by the holding electrode 4. That is, the PSG film 14 is formed. The flow of PH_3 is controlled so that the amount of P that is included in the PSG film 14 is 4 weight%, for example, and the reaction time, that is, the time high-frequency power is applied, is controlled so that the film thickness becomes 1 μm, for example (FIG. 1a).

The PSG film 14 formed on the surface of the quartz substrate 3 at this time is not dense since the temperature of the quartz substrate 3 at the time of film formation is as low as 350 °C. However, the amount of impurities contained is sufficiently small, since highly dense reactive gases SiH_4, O_2, and PH_3 are used, and there is no contamination from the inner wall, the opposing electrode 6 or the like owing to the temperature as low as 350 °C in the film formation chamber 1.

When the residual gas is exhausted by the exhaust pipe 9 and the degrees of vacuum in the film formation chamber 1 and the preliminary exhaust chamber 2 become equal to each other, the door 13 provided on the partition wall between these two spaces opens, the semiconductor substrate holder 11 on which the semiconductor substrates 10 are placed is carried from the preliminary exhaust chamber 2 to the film formation chamber, and each semiconductor substrate 10 is set so as to oppose to each of the quartz substrates 3 under the holding electrode 4.

Ar gas is introduced from an Ar gas introducing port 8, and high-frequency

power is applied between the sputtering electrode 5 and the holding electrode 4 incorporating the magnet. At this time, sputtering using the quartz substrate 3 on the surface of which the PSG film 14 is formed, used as a target, is performed. Si, O, and P atoms which constitute the PSG film 14 are knocked out by accelerated Ar ions, fly to the surface of the semiconductor substrate 10 which is positioned so as to oppose to the target, and a PSG film 15 is formed again on the surface of the semiconductor substrate 10.

When the PSG film 15 with a desired thickness such as 0.5 μm, for example, is formed, high-frequency power and Ar gas are stopped, and the residual gas is discharged from the exhaust port 9. After that, the door 13 opens and the semiconductor substrate holder 11 on which the semiconductor substrates 10 are placed is carried from the film formation chamber 1 to the preliminary chamber 2 and taken outside.

When the PSG film 15 is formed by a sputtering method in the above-described way, Si, O, and P atoms knocked out from the quartz substrate 3 as a target have sufficiently high energy. Therefore, the PSG film 15 which is formed on the surface of the semiconductor substrate 10 where an underlying wiring is formed has good step coverage over the underlying wiring, and is dense enough to block moisture, impurities or the like from entering from the outside. In addition, the concentration of P in the PSG film 15 which determines the gettering effect with respect to alkali ions deteriorating the characteristics of the semiconductor device can be precisely controlled by controlling the PH_3 flow at the time of forming the PSG film 14 on the surface of the quartz substrate 3 by a CVD method. Furthermore, a highly pure reactive gas is used when forming the PSG film 14 on the surface of the quartz substrate 3 by a CVD method, and the temperature when forming the PSG film 15 by a CVD method or a sputtering method is low, so that impurities from the outside do not enter. Accordingly, the PSG film 15 has a significant feature that the content of impurities, which adversely affect the characteristics of a semiconductor device, is small. In this way, since an interlayer insulating film with good characteristics can be formed without performing heat treatment at high temperature, manufacture of a highly reliable LSI with high

density becomes easy.

In addition, in this embodiment, when the PSG film 15 is formed on the surface of the quartz substrate 3 by a CVD method, a PSG film is also formed on the inner wall of the film formation chamber 1. Therefore, impurities such as metal ions can be prevented from coming out from the inner wall of the film formation chamber 1, when forming the PSG film on the surface of the semiconductor substrate 10 by a sputtering method later. Accordingly, this embodiment also has an advantage that the PSG film formed on the semiconductor substrate 10 is not contaminated.

In the above-described embodiment, when forming the PSG film 14 on the surface of the quartz substrate 13 by a CVD method, a plasma-enhanced CVD method in which a reactive gas is excited by high frequency power is used; however, a CVD method in which thermal decomposition reaction is used or a photo-excited CVD method in which a reactive gas is excited by ultraviolet radiation may be used. In addition, as for a thin film formation apparatus, it is not necessarily required that a CVD method and a sputtering method are performed in the same film formation chamber 1 as in the embodiment. The quartz substrate 3 on which the PSG film 14 is formed by a CVD method may be carried to an adjacent chamber so that the PSG film 15 is formed on the surface of the semiconductor substrate 10 by a sputtering method there. Furthermore, as long as contamination from the outside is fully considered, after the PSG film is formed on the surface of the quartz substrate by a CVD method, the PSG film 15 may be formed on the surface of a semiconductor substrate 11 with the use of the quartz substrate 3 as a target in another sputtering apparatus.

Although the method and apparatus for forming a PSG film used as an interlayer insulating film of a semiconductor device have been described above, the manufacturing method according to the present invention has great effects also in a case where a refractory metal thin film is formed for forming a gate electrode. Refractory metals such as Mo are expected as a gate electrode material of a high-density and high-speed LSI, since their electric resistance is two digits smaller, compared to polycrystalline Si which is conventionally used as a gate electrode. However, in a case where a thin film is formed by a sputtering method, a highly pure target is hard to be

obtained; and therefore, it is difficult to form a refractory metal thin film in which the amount of alkali ions and other impurities contained is small. And this is a major obstacle to the use of a refractory metal as a gate electrode. Thus, by using the thin film formation method of the present invention, a target having a refractory metal thin film in which the amount of impurities contained is small can be easily obtained, and a refractory metal thin film in which the amount of impurities contained is small can be formed by a sputtering method; therefore, a high-density and high-speed LSI with high reliability can be manufactured with a high yield.

Effects of the Invention

A dense thin film in which the amount of impurities contained adversely affecting a semiconductor device is small and which has sufficiently good characteristics even without conducting heat treatment at high temperature can be formed.

4. Brief Description of the Drawings

FIG. 1 and FIG. 2 are schematic cross-sectional views of a thin film formation apparatus for describing the thin film formation method of the present invention.

3: quartz substrate, 4: holding electrode used when forming a thin film by a CVD method and a sputtering method, 5: electrode used in sputtering, 6: opposing electrode used in performing a plasma-enhanced CVD method, 10: semiconductor substrate, 14: thin film formed on the surface of a quartz substrate by a CVD method, 15: thin film formed by a sputtering method

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭59—68921

⑤Int. Cl.³	識別記号	庁内整理番号
H 01 L 21/20		7739—5F
21/203		7739—5F
21/205		7739—5F
21/285		7638—5F

⑬公開　昭和59年(1984)4月19日

発明の数　1

審査請求　未請求

（全 4 頁）

⑭薄膜の形成方法

⑳特　　願　昭57—179405

㉒出　　願　昭57(1982)10月12日

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1、発明の名称

薄膜の形成方法

2、特許請求の範囲

基板の表面に気相化学堆積法により膜を形成した後、前記基板をターゲットとするスパッタリング法により半導体基板に所定の厚さの薄膜を形成することを特徴とする薄膜の形成方法。

3、発明の詳細な説明

産業上の利用分野

本発明は半導体装置の製造工程における薄膜の形成方法に関する。

従来例の構成とその問題点

半導体装置，例えばＭＯＳＬＳＩの製造工程において絶縁体，半導体あるいは金属の薄膜が何度か形成されるが、その形成方法は薄膜の種類に応じて大気圧下又は減圧下におけるＣＶＤ法（chemical vapor deposition：気相化学堆積法），真空蒸着法，スパッタリング法等が選ばれる。たとえばＳｉゲートＭＯＳＬＳＩの製造工程においては多結晶Ｓｉよりなる第1層配線とＡｌよりなる第2層配線間の層間絶縁膜としてＳｉO₂膜やＰＳＧ（リンケイ酸ガラス）膜がＣＶＤ法で形成される。

ＣＶＤ法で形成されたＳｉO₂膜やＰＳＧ膜は重金属やアルカリイオン等ＭＯＳＬＳＩの特性に悪影響を及ぼす不純物の含有量が少ない。これはガスの精製が容易なためＣＶＤ法ではＳｉH₄，O₂やPRs等高純度の反応ガスを用いるためである。一方ＣＶＤ法は基板たとえば４５０℃で薄膜を形成するためにこの薄膜は基板への密着力が弱く緻密さが不十分である。したがって密着力を強化し緻密にして層間絶縁膜として十分な特性をもたせるためには１０００℃に近い高温での熱処理を施す必要がある。

ＬＳＩの高密度化が進み微細寸法のＭＯＳトランジスタを形成するためにはソース，ドレインの接合深さを浅くする必要がある。たとえばゲート長が1.5 μm のＭＯＳトランジスタを形成するにはソース，ドレインの接合深さを0.3 μm 程度に

する必要があり、ソース，ドレイン領域にイオン注入でBを添加した後は、従来の１０００℃という高温の熱処理を施すことができない。そのため層間絶縁膜としてＣＶＤ法で形成しただけのSiO₂膜やＰＳＧ膜は、緻密さが不十分なため層間絶縁膜として必要な絶縁耐圧あるいは不純物阻止能かアルカリイオン補強力などが劣る。

またＬＳＩの層間絶縁膜としてＣＶＤ法で形成した前記のSiO₂膜やＰＳＧ膜は下部配線上でのステップカバレッジが悪い。そのためにこれらSiO₂膜かＰＳＧ膜上に形成した上部配線は下部配線と交差する部分で厚さが小となったり、エッチングによるパターン形成の際に線幅が細くなったり、さらにひどくなると断線さえも生じやすくなる。この問題を解決するために層間絶縁膜に高濃度のリンを含むＰＳＧ膜を形成し１０００℃のリンを含む雰囲気中で熱処理を施して流動させる、いわゆるリフロー処理を行っていた。しかしなから６の１０００℃の高温の熱処理であるリフロー処理も前述のように浅いソース，ドレイン接合を

１の基板に薄膜を形成しひき続いてこの薄膜が形成された第１の基板をターゲットとしてスパッタリング法により対向して置かれた半導体基板の表面に所望の厚さの薄膜を形成することを特徴とするものである。

すでに述べたようにＣＶＤ法で第１の基板に形成した薄膜は純度の高い反応ガスを用いることによって不純物含有量を十分に少なくすることができる。

一方、スパッタリング法ではターゲットから解離した原子は高いエネルギーを有している。これは高電界で加速された高エネルギーのArイオンによりターゲット表面からたたき出されたためで、この高エネルギーの原子が半導体基板表面に付着することにより形成された薄膜は半導体基板への密着力が強く高温の熱処理を施さなくても十分な緻密さを有している。

したがって本発明は上述のように特性の良い薄膜をスパッタリング法で形成する際に、不純物含有量の少ない薄膜がＣＶＤ法で表面に形成された形成するためには行なうことができず、したがって高密度のＬＳＩ製造においては上部配線の細りか断線等の問題が生ずることが多い。

以上に述べたように高温の熱処理を施すことができない高密度ＬＳＩの製造工程においては従来のＣＶＤ法で形成した層間絶縁膜は製造歩留りや信頼性の低下の大きな原因となる。

発明の目的

本発明は不純物の含有量が少なく、さらに高温で熱処理を施さなくても十分に特性の良い薄膜を形成する方法および薄膜形成装置を提供することを目的とする。

発明の構成

薄膜の形成方法の一つにスパッタリング法がある。これはたとえばArイオンを高電界で加速しターゲットに衝突させてターゲットを構成する原子を解離させターゲットに対向して置かれたたとえば半導体基板に付着させることにより薄膜を形成するものである。

本発明の薄膜形成方法は、前述のＣＶＤ法で第１の基板を、しかもこの薄膜が形成されたあと外部から汚染されることなく半導体基板に対向させてターゲットとして用いるものである。

実施例の説明

以下に本発明の一実施例を説明する。

本実施例での薄膜形成装置の断面図を第１図に示す。

第１図に示す薄膜形成装置は膜形成室１と予備排気室２を有している。膜形成室１内には第１の基板たとえば石英基板３と、これを保持し、保持する石英基板３を加熱するための加熱装置及びスパッタ時に電子を加速するための陽石を内蔵する保持電極４、スパッタ用電極５、対向電極６が設けられ、さらにＣＶＤ用の反応ガス導入管７、スパッタ用のArガス導入管８と薄膜成室１内を排気するために排気ポンプにつながる排気管９が接続されている。

予備排気室２には半導体基板１０を収容した半導体基板保持具１１があり、排気ポンプにつながる排気管１２が接続されている。また膜形成室１

と予備排気室２との隔壁には扉１３が設けられており、この扉１３を開けて半導体基板１０を載置して半導体基板保持具１１を予備排気室２から膜形成室１に移るいはその逆方向に搬送するための搬送装置も設けられている。

この様な膜形成装置を用いて半導体基板１０の表面にＰＳＧ膜を形成する場合について説明する。

複数の半導体基板１０が半導体基板保持具１１に載置されて予備排気室２に置かれる。扉１３が閉じられ排気管１２につながった排気ポンプにより予備排気室２内が排気される。

一方膜形成室１内では第１の基板である石英基板３表面にＰＳＧ膜１４がＣＶＤ法で形成される。まず膜形成室１が排気管９につながる排気ポンプで真空度が10^{-3}Torr になるまで排気され、その間に保持電極４に保持された石英基板３は保持電極４の加熱装置により３５０℃になるまで加熱される。その後反応ガス導入管７から反応ガスであるSiH_4，O_2，PH_3が導入され膜形成室１内の真空度が１０Torr に安定した後、対向電極５と保持電極４間に高周波電力が印加される。両電極間では反応ガス分子が高周波電力により励起されガス間の反応が起りやすくなる。その結果、保持電極４に保持され加熱された石英基板３の表面にPH_3ガスより分解した P を含むSiH_4とO_2との反応により形成されたSiO_2膜、すなわちＰＳＧ膜１４が形成される。ＰＳＧ膜１４に含まれるＰの量は例えば４重量％になるようPH_3の流量を制御し、膜厚は例えば１ μm になるように反応時間すなわち高周波電力の印加時間を制御する（第１図a）。

この時に石英基板３表面に形成されたＰＳＧ膜１４は膜形成時の石英基板３の温度が３５０℃と低いために緻密ではないが高密度の反応ガスSiH_4，O_2，PH_3を用いること、膜形成室１内の温度が３６０℃以下と低いため内壁や対向電極５等から汚染されることもないため、不純物の含有量は十分に少なくなっている。

残留ガスが排気管９より排気され膜形成室１と予備排気室２との真空度が等しくなると、これら二つの空間の隔壁に設けられた扉１３が開いて半導体基板１０が載置された半導体基板保持具１１が予備排気室２から膜形成室に搬送され、保持電極４の下方において、各半導体基板１０が石英基板３の各々に対向するように置かれる。

Ar ガス導入口８より Ar ガスが導入され、磁石を内蔵する保持電極４とスパッタ用電極５の間に高周波電力が印加される。この時に表面にＰＳＧ膜１４が形成された石英基板３をターゲットとするスパッタリングが行なわれ、ＰＳＧ膜１４を構成する Si，O，P 原子が加速された Ar イオンによりたたき出され、ターゲットと対向して位置する半導体基板１０表面に飛来し、再びこの半導体基板１０表面にＰＳＧ膜１５が形成される。

所望の膜厚例えば0.6 μm のＰＳＧ膜１５が形成されると高周波電力と Ar ガスがきられ、残留ガスが排気口９より排出された後扉１３が開いて半導体基板１０が載置された半導体基板保持具１１は膜形成室１から予備室２に搬送され外に取出される。

以上に述べた方法でスパッタリング法によりＰＳＧ膜１５が形成される際に、ターゲットである石英基板３よりたたき出された Si，O，P 原子は十分高いエネルギーを有しているため下部配線が形成された半導体基板１０の表面に形成されたＰＳＧ膜１５は下部配線上のステップカバレッジが良く、外部から水分や不純物等が侵入するのを阻止するに十分な緻密さをもっている。また半導体装置の特性を劣化させるアルカリイオンに対するゲッタリング効果を決めるＰＳＧ膜１５中のＰ濃度はＣＶＤ法で石英基板３表面にＰＳＧ膜１４を形成する際のPH_3流量を制御することにより精密に制御することができる。さらにＣＶＤ法で石英基板３表面にＰＳＧ膜１４を形成する際に高純度の反応ガスを用いており、またＣＶＤ法やスパッタリング法でＰＳＧ膜１５を形成する際の温度が低いため外部から不純物の侵入することがなく、ＰＳＧ膜１５は半導体装置の特性に悪影響を及ぼす不純物の含有量が少ないという大きな特長を有している。このように高温の熱処理を施すことな

く特性の良い層間絶縁膜が形成できるために、高密度でかつ信頼性の高いＬＳＩの製造が容易になる。

また本実施例ではＣＶＤ法で石英基板３表面にＰＳＧ膜１５を形成する際に、膜形成室１内壁にもＰＳＧ膜が形成され、そのために後で半導体基板１０表面にＰＳＧ膜をスパッタリング法で形成する際に膜形成室１内壁から金属イオンなどの不純物が出るのを防げるため、半導体基板１０が形成されたＰＳＧ膜が汚染されることがないという長所もわわせもっている。

以上に述べた実施例ではＣＶＤ法で石英基板３表面にＰＳＧ膜１４を形成するのに高周波電力で反応ガスを励起するプラズマＣＶＤ法を用いているが、熱分解反応を用いるＣＶＤ法あるいは紫外光で反応ガスを励起する光ＣＶＤ法を用いても良い。また薄膜形成装置は実施例のようにＣＶＤ法とスパッタリング法を同一の膜形成室１内で行う必要はなく、ＣＶＤ法でＰＳＧ膜１４が形成された石英基板３が隣接するチャンバーに搬送されて

として用いることの大きな障害となっている。そこで、本発明の薄膜の形成方法を用いると容易に不純物の含有量が少ない高融点金属薄膜を有するターゲットが得られ、不純物含有量の少ない高融点金属薄膜がスパッタリング法で形成できるので高密度、高速度かつ高信頼性のＬＳＩを高歩留りで製造することができる。

発明の効果

半導体装置に悪影響を及ぼす不純物の含有量が少なく、かつ高温での熱処理を施さなくても十分特性の良い緻密な薄膜を形成することができる。

4、図面の簡単な説明

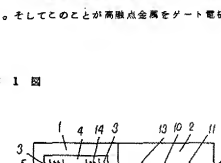
第１図、第２図は本発明の薄膜の形成方法を説明するための薄膜形成装置の概略断面図である。

３……石英基板、４……ＣＶＤ法およびスパッタリング法で薄膜を形成する際の保持基板、５……スパッタリング時の電極、８……プラズマＣＶＤ法を行う場合の対向電極、１０……半導体基板、１４……ＣＶＤ法で石英基板表面に形成した薄膜、１５……スパッタリング法で形成した薄膜。

そこで半導体基板１０表面へスパッタリング法でＰＳＧ膜１５が形成されても良い。さらには、外部からの汚染が十分考慮されておれば、ＣＶＤ法で石英基板表面にＰＳＧ膜を形成した後、他のスパッタリング装置にこの石英基板３をターゲットとして用いて半導体基板１１表面にＰＳＧ膜１５を形成してもよい。

以上は半導体装置の薄間絶縁膜として用いるＰＳＧ膜を形成する方法と装置について説明してきたが、ゲート電極を形成するために高融点金属薄膜を形成する場合にも本発明の製造方法は大きな効果を有する。Ｍｏ等の高融点金属は、従来ゲート電極として用いられている多結晶 Si に比べ、電気抵抗が２桁も小さいため高密度、高速度のＬＳＩのゲート電極材料として期待されている。しかしながら薄膜形成をスパッタリング法により形成する場合に高純度のターゲットが得がたく、そのためアルカリイオンをはじめとする不純物含有量の少ない高融点金属薄膜を形成するのが困難である。そしてこのことが高融点金属をゲート電極

第 1 図



第 2 図